

D100N10ES

Perfect MOS N-MOSFET 100V, 5mΩ, 100A



重庆平伟实业股份有限公司

Features

- Uses PingWei advanced PerfectMOS technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- Excellent Low Ciss
- Qualified according to JEDEC criteria

Benefits

- High robustness and reliability
- Increases maximum current capability
- Low power loss, high power density
- Easy paralleling

Applications

- Synchronous Rectification for AC/DC Quick Charger
- Battery management
- UPS (Uninterruptible Power Supplies)

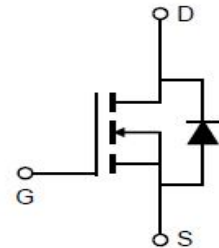
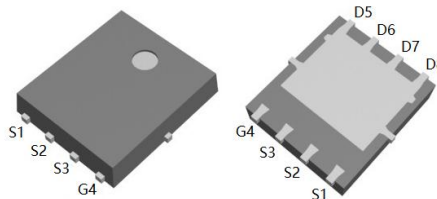


100% DVDS Tested
100% Avalanche Tested

Product Summary

V_{DS}	100V
$R_{DS(on)@10V}$ typ	5mΩ
I_D	100A

DFN5*6



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
D100N10ES	D100N10ES	DFN5x6	Tape&Reel	13 inches	12mm	5000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	100	V
Continuous drain current	I_D	111	A
$T_C = 25^\circ\text{C}$ (Silicon limit)		100	
$T_C = 25^\circ\text{C}$ (Package limit)		70	
$T_C = 100^\circ\text{C}$ (Silicon limit)		12	
$T_a = 25^\circ\text{C}$			
Pulsed drain current ($T_C = 25^\circ\text{C}$, $t_p = 100\mu\text{s}$)	$I_{D\ pulse}$	400	A
Avalanche energy, single pulse ($L=0.5\text{mH}$, $V_{ds}=50\text{V}$)	E_{AS}	90	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation	P_{tot}	128	W
$T_C = 25^\circ\text{C}$		1.6	
$T_a = 25^\circ\text{C}$			
Operating junction and storage temperature	T_j, T_{stg}	-55...+150	$^\circ\text{C}$
Soldering temperature, wave soldering only allowed at leads (1.6mm from case for 10s)	T_{sold}	260	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance, junction – case.	RthJC	-	-	1.0	°C/W	-
Thermal resistance, junction - ambient(min. footprint)	RthJA	-	-	80	°C/W	-

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV_{DSS}	100	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{GS(th)}$	2.0	-	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	0.02	1	μA	$V_{DS}=100V, V_{GS}=0V$ $T_j=25^\circ C$ $T_j=150^\circ C$
Gate-source leakage current	I_{GSS}	-	± 10	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	5.0	6.0	mΩ	$V_{GS}=10V, I_D=50A$
Transconductance	g_{fs}	-	55	-	S	$V_{DS}=5V, I_D=50A$

Dynamic Characteristic

Input Capacitance	C_{iss}	-	2509	-	pF	$V_{GS}=0V, V_{DS}=50V,$ $f=1MHz$
Output Capacitance	C_{oss}	-	543	-		
Reverse Transfer Capacitance	C_{rss}	-	26	-		
Gate Total Charge	Q_G	-	41	-	nC	$V_{DS}=50V, I_D=50A,$ $V_{GS}=10V$
Gate-Source charge	Q_{gs}	-	15	-		
Gate-Drain charge	Q_{gd}	-	10	-		
Turn-on delay time	$t_{d(on)}$	-	16.8	-	ns	$V_{GS}=10V, V_{DD}=50V,$ $R_{G_ext}=1.6\Omega, I_D=50A$
Rise time	t_r	-	56.4	-		
Turn-off delay time	$t_{d(off)}$	-	32	-		
Fall time	t_f	-	11	-		
Gate resistance	R_G	-	1.6	-	Ω	$V_{GS}=0V, V_{DS}=0V,$ $f=1MHz$

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Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	-	1.2	V	$V_{GS}=0V, I_{SD}=50A$
Body Diode Continuous Forward Current	I_S	-	-	100	A	$TC = 25^{\circ}C$
Body Diode Pulsed Current	I_S pulse	-	-	400	A	$TC = 25^{\circ}C$
Body Diode Reverse Recovery Time	t_{rr}	-	48	-	ns	$I_F=50A, dI/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	-	54	-	nC	



Typical Performance Characteristics

Fig 1: Output Characteristics

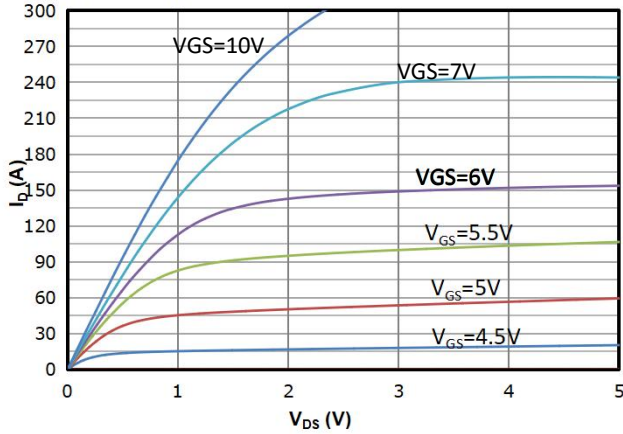


Fig 2: Transfer Characteristics

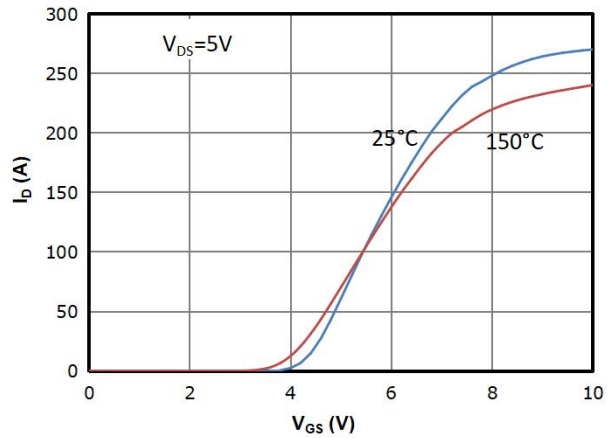


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

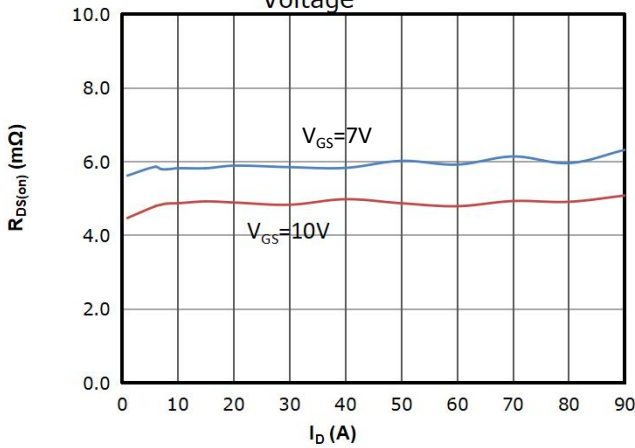


Fig 4: $R_{DS(on)}$ vs Gate Voltage

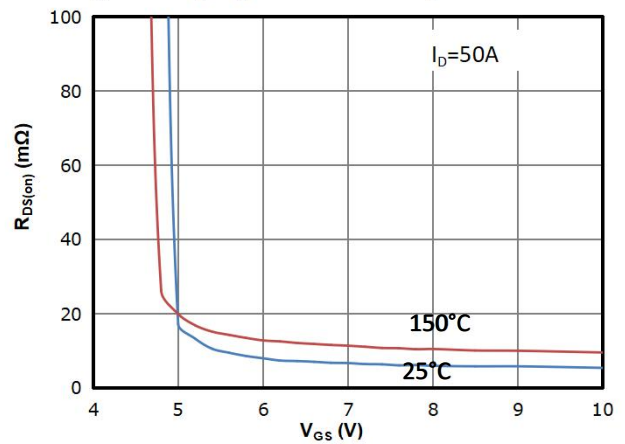


Fig 5: $R_{DS(on)}$ vs. Temperature

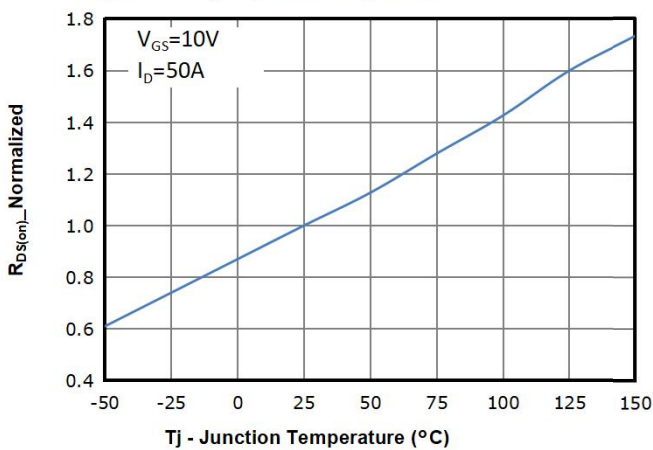


Fig 6: $V_{GS(th)}$ vs. Temperature

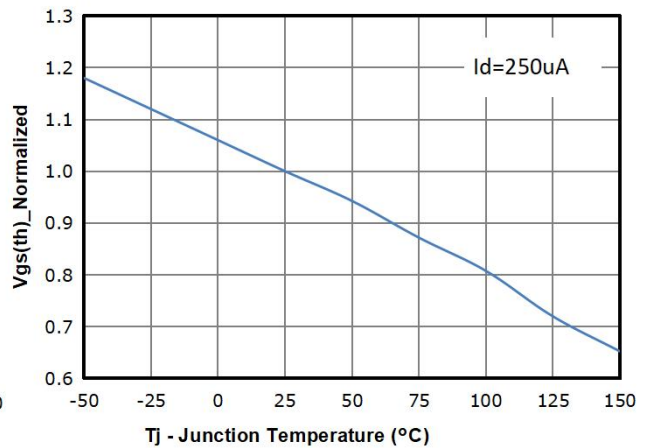




Fig 7: BVdss vs. Temperature

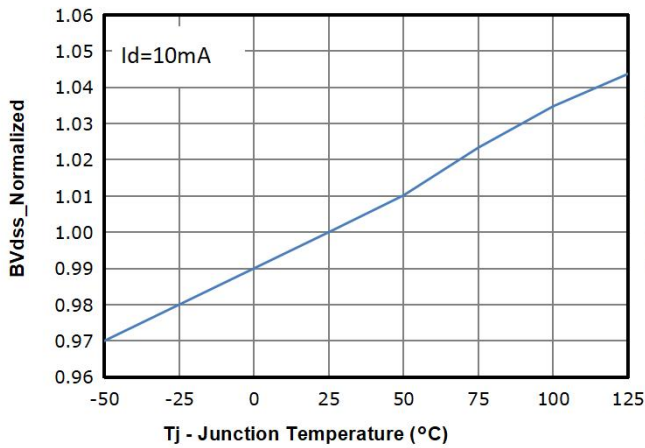


Fig 8: Capacitance Characteristics

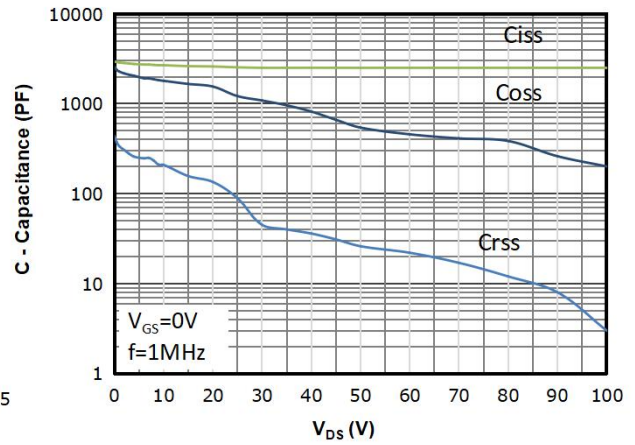


Fig 9: Gate Charge Characteristics

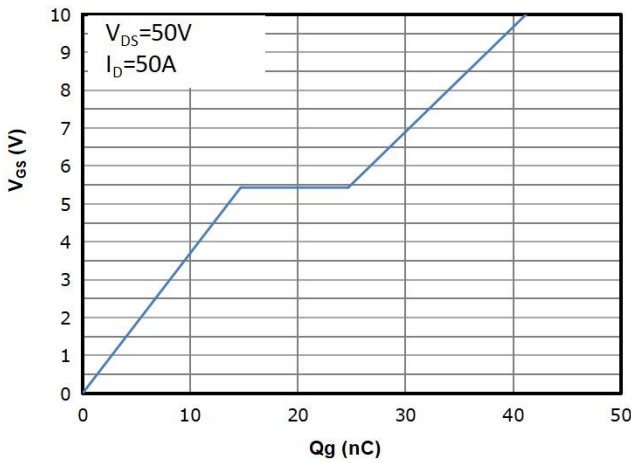


Fig 10: Body-diode Forward Characteristics

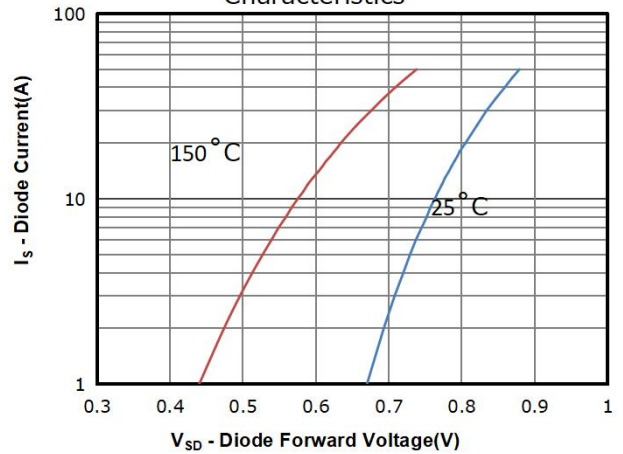


Fig 11: Power Dissipation

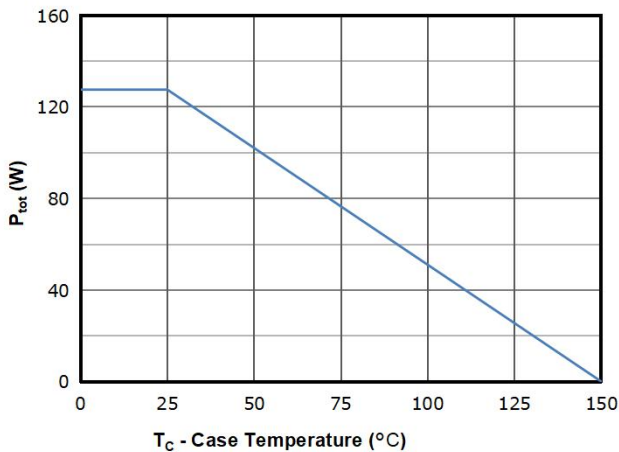


Fig 12: Drain Current Derating

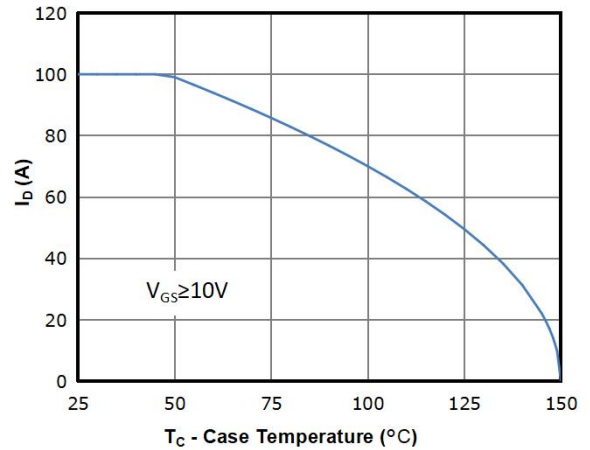




Fig 13: Safe Operating Area

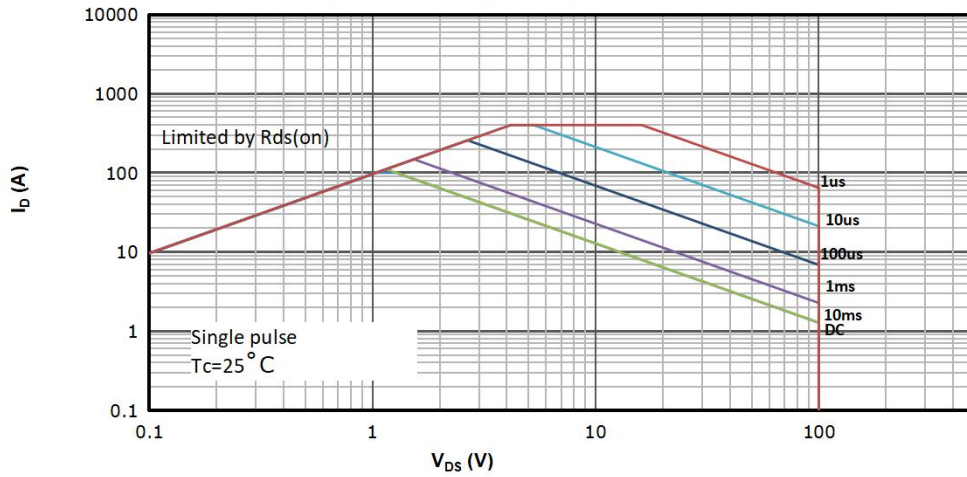
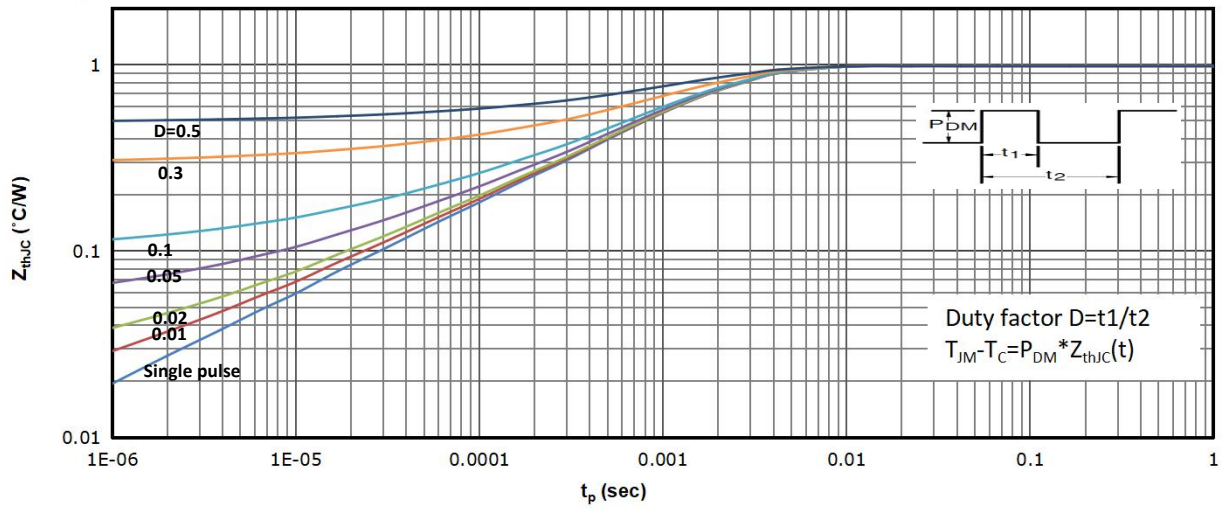
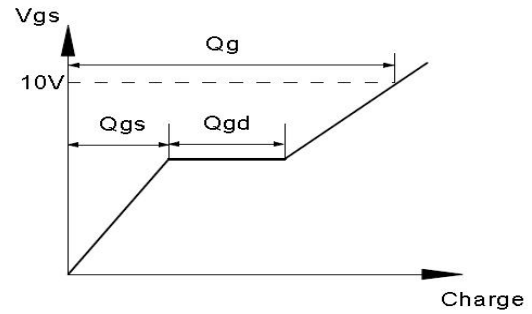
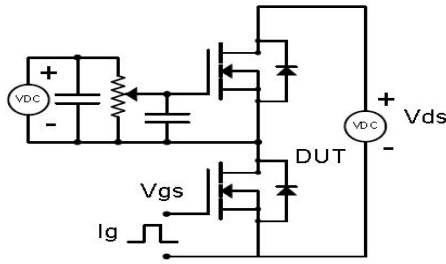


Fig 14: Max. Transient Thermal Impedance

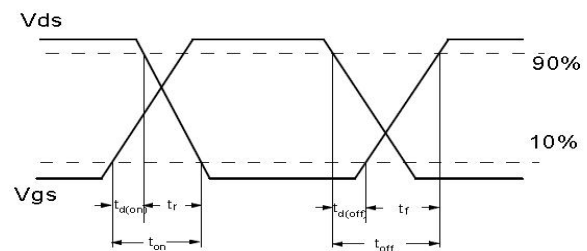
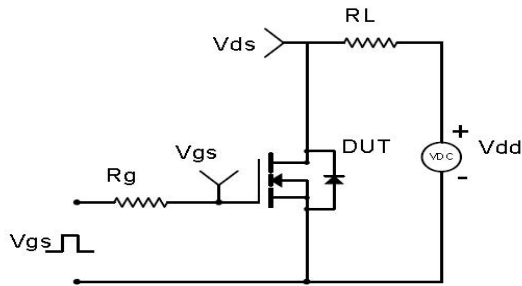


Test Circuit & Waveform

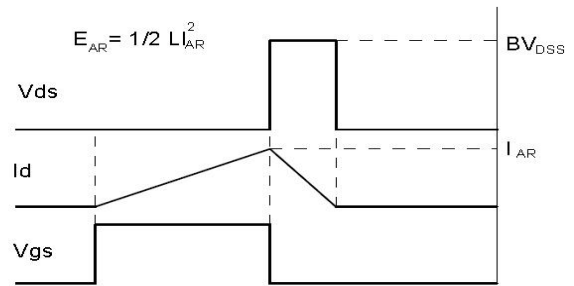
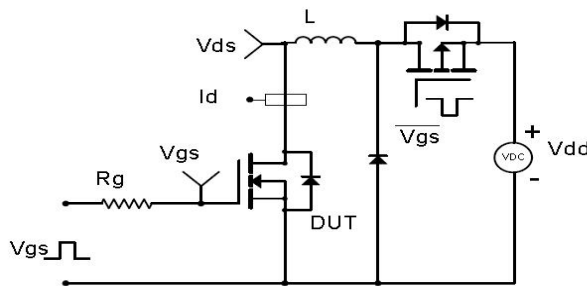
Gate Charge Test Circuit & Waveform



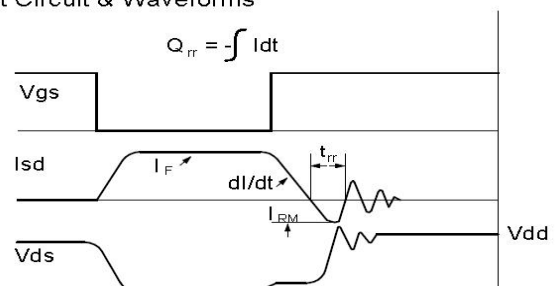
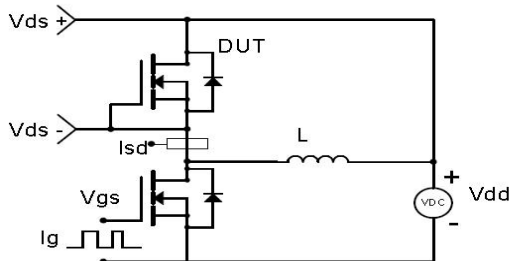
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



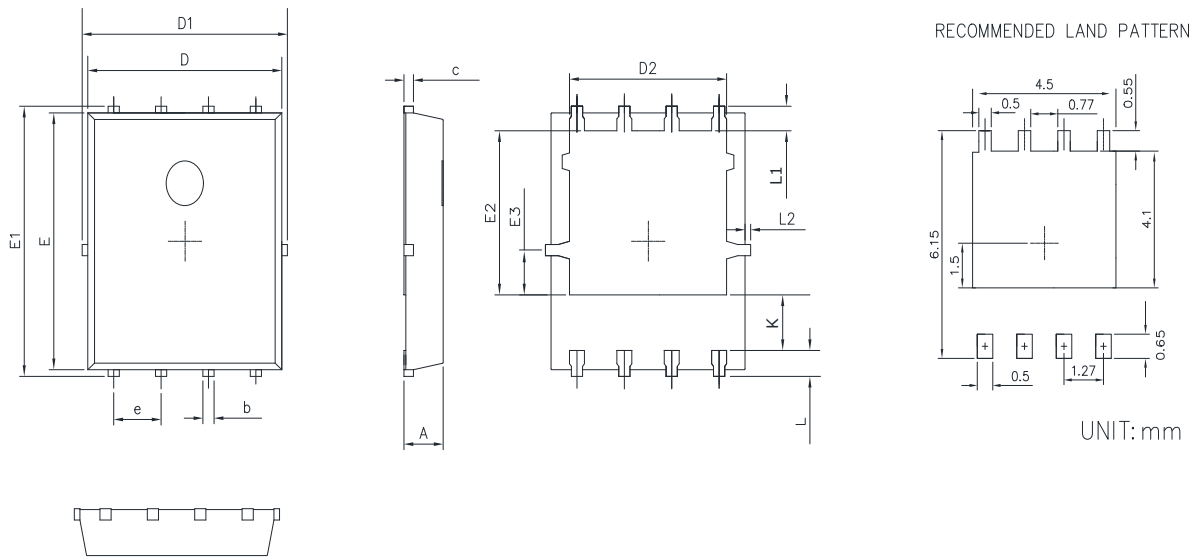
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Package Outline: DFN5*6



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.25	0.50	0.010	0.020
c	0.10	0.30	0.004	0.012
D	4.80	5.30	0.189	0.209
D1	4.90	5.50	0.193	0.217
D2	3.92	4.20	0.154	0.165
E	5.65	5.85	0.222	0.230
E1	5.90	6.20	0.232	0.244
E2	3.33	3.78	0.131	0.149
E3	0.80	1.00	0.031	0.039
e	1.27		0.050	
L	0.40	0.70	0.016	0.028
L1	0.65		0.026	
L2	0.00	0.15	0.000	0.006
K	1.00	1.50	0.039	0.059



Revision History

Revision	Date	Major changes
1.0	2023/7/10	Release of Formal Version.

Disclaimer

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